

NAME

gbz80 — CPU opcode reference uwu

DESCRIPTION

hOi!! Here's the opcodes supported by that dang ol' *rgbasm*(1) along with some details, the number of bytes and stuff ya need to encode them, and how many CPU cycles at 1MHz (or 2MHz in that **NASTY** GBC dual speed mode) needed to make 'em do the thing!

Note: All GROSS MATH STUFF that uses register (\hat{A}) as destination can omit the destination as it is assumed to be register (\hat{A}) by default. The following two lines have the same effect:

```
OR ( $\hat{A}$ ), =B
OR =B
```

LEGEND

Here's some words and what they mean!

- r8* One of those 8-bit registers (\hat{A} , \hat{B} , \hat{C} , \hat{D} , \hat{E} , \hat{H} , \hat{L})
- r16* One of those general-purpose 16-bit registers (\hat{BC} , \hat{DE} , \hat{HL})
- n8* 8-bit number
- n16* 16-bit number
- e8* 8-bit offset (-128 to 127)
- u3* Weird 3-bit number (0 to 7)
- cc* Condition codes:
Z Do thing if Z is set
NZ Do thing if Z is not set
C Do thing if C is set
NC Do thing if C is not set
!cc Do the opposite thing
- vec* One of those dumb **RST** vectors (0x00, 0x08, 0x10, 0x18, 0x20, 0x28, 0x30, and 0x38)

INSTRUCTION OVERVIEW**8-bit Math and Logic Doodads**

- “ADC (\hat{A}), *r8*”
- “ADC (\hat{A}), [*D*], *e8*”
- “ADC (\hat{A}), *n8*”
- “ADD (\hat{A}), *r8*”
- “ADD (\hat{A}), [*D*], *e8*”
- “ADD (\hat{A}), *n8*”
- “AND (\hat{A}), *r8*”
- “AND (\hat{A}), [*D*], *e8*”
- “AND (\hat{A}), *n8*”
- “CP (\hat{A}), *r8*”
- “CP (\hat{A}), [*D*], *e8*”
- “CP (\hat{A}), *n8*”
- “DEC *r8*”
- “DEC [*D*], *e8*”
- “INC *r8*”
- “INC [*D*], *e8*”
- “OR (\hat{A}), *r8*”
- “OR (\hat{A}), [*D*], *e8*”

“OR ($\hat{a}\hat{c}\hat{l}$),n8”
 “SBC ($\hat{a}\hat{c}\hat{l}$),r8”
 “SBC ($\hat{a}\hat{c}\hat{l}$),[$\hat{D}\hat{2}\hat{a}$ ($\hat{a}\hat{a}$)i $\hat{4}_i$]”
 “SBC ($\hat{a}\hat{c}\hat{l}$),n8”
 “SUB ($\hat{a}\hat{c}\hat{l}$),r8”
 “SUB ($\hat{a}\hat{c}\hat{l}$),[$\hat{D}\hat{2}\hat{a}$ ($\hat{a}\hat{a}$)i $\hat{4}_i$]”
 “SUB ($\hat{a}\hat{c}\hat{l}$),n8”
 “XOR ($\hat{a}\hat{c}\hat{l}$),r8”
 “XOR ($\hat{a}\hat{c}\hat{l}$),[$\hat{D}\hat{2}\hat{a}$ ($\hat{a}\hat{a}$)i $\hat{4}_i$]”
 “XOR ($\hat{a}\hat{c}\hat{l}$),n8”

16-bit Math Things

“ADD $\hat{D}\hat{2}\hat{a}$ ($\hat{a}\hat{a}$)i $\hat{4}_i$,r16”
 “DEC r16”
 “INC r16”

Bit Opurrations >=3c

“BIT u3,r8”
 “BIT u3,[$\hat{D}\hat{2}\hat{a}$ ($\hat{a}\hat{a}$)i $\hat{4}_i$]”
 “RES u3,r8”
 “RES u3,[$\hat{D}\hat{2}\hat{a}$ ($\hat{a}\hat{a}$)i $\hat{4}_i$]”
 “SET u3,r8”
 “SET u3,[$\hat{D}\hat{2}\hat{a}$ ($\hat{a}\hat{a}$)i $\hat{4}_i$]”
 “SWAP r8”
 “SWAP [$\hat{D}\hat{2}\hat{a}$ ($\hat{a}\hat{a}$)i $\hat{4}_i$]”

Shifty Bit Stuff \hat{o}

“RL r8”
 “RL [$\hat{D}\hat{2}\hat{a}$ ($\hat{a}\hat{a}$)i $\hat{4}_i$]”
 “RLA”
 “RLC r8”
 “RLC [$\hat{D}\hat{2}\hat{a}$ ($\hat{a}\hat{a}$)i $\hat{4}_i$]”
 “RLCA”
 “RR r8”
 “RR [$\hat{D}\hat{2}\hat{a}$ ($\hat{a}\hat{a}$)i $\hat{4}_i$]”
 “RRA”
 “RRC r8”
 “RRC [$\hat{D}\hat{2}\hat{a}$ ($\hat{a}\hat{a}$)i $\hat{4}_i$]”
 “RRCA”
 “SLA r8”
 “SLA [$\hat{D}\hat{2}\hat{a}$ ($\hat{a}\hat{a}$)i $\hat{4}_i$]”
 “SRA r8”
 “SRA [$\hat{D}\hat{2}\hat{a}$ ($\hat{a}\hat{a}$)i $\hat{4}_i$]”
 “SRL r8”
 “SRL [$\hat{D}\hat{2}\hat{a}$ ($\hat{a}\hat{a}$)i $\hat{4}_i$]”

Load Stuff

“LD r8,r8”
 “LD r8,n8”
 “LD r16,n16”
 “LD [$\hat{D}\hat{2}\hat{a}$ ($\hat{a}\hat{a}$)i $\hat{4}_i$],r8”
 “LD [$\hat{D}\hat{2}\hat{a}$ ($\hat{a}\hat{a}$)i $\hat{4}_i$],n8”
 “LD r8,[$\hat{D}\hat{2}\hat{a}$ ($\hat{a}\hat{a}$)i $\hat{4}_i$]”
 “LD [r16],($\hat{a}\hat{c}\hat{l}$)”

“LD [n16],($\hat{a}\hat{c}\hat{l}\hat{A}\hat{a}\hat{c}\hat{l}$)”
 “LDH [n16],($\hat{a}\hat{c}\hat{l}\hat{A}\hat{a}\hat{c}\hat{l}$)”
 “LDH [$\hat{a}\hat{c}\hat{l}\hat{A}\hat{a}\hat{c}\hat{l}$],($\hat{a}\hat{c}\hat{l}\hat{A}\hat{a}\hat{c}\hat{l}$)”
 “LD ($\hat{a}\hat{c}\hat{l}\hat{A}\hat{a}\hat{c}\hat{l}$),[r16]”
 “LD ($\hat{a}\hat{c}\hat{l}\hat{A}\hat{a}\hat{c}\hat{l}$),[n16]”
 “LDH ($\hat{a}\hat{c}\hat{l}\hat{A}\hat{a}\hat{c}\hat{l}$),[n16]”
 “LDH ($\hat{a}\hat{c}\hat{l}\hat{A}\hat{a}\hat{c}\hat{l}$),[$\hat{a}\hat{c}\hat{l}\hat{A}\hat{a}\hat{c}\hat{l}$ C]”
 “LD [$\hat{D}\hat{1}\hat{2}\hat{a}$ ($\acute{a}\hat{a}\hat{a}$)i $\hat{1}\hat{4}\hat{i}$],($\hat{a}\hat{c}\hat{l}\hat{A}\hat{a}\hat{c}\hat{l}$)”
 “LD [$\hat{D}\hat{1}\hat{2}\hat{a}$ ($\acute{a}\hat{a}\hat{a}$)i $\hat{1}\hat{4}\hat{i}$],($\hat{a}\hat{c}\hat{l}\hat{A}\hat{a}\hat{c}\hat{l}$)”
 “LD ($\hat{a}\hat{c}\hat{l}\hat{A}\hat{a}\hat{c}\hat{l}$),[$\hat{D}\hat{1}\hat{2}\hat{a}$ ($\acute{a}\hat{a}\hat{a}$)i $\hat{1}\hat{4}\hat{i}$]”
 “LD ($\hat{a}\hat{c}\hat{l}\hat{A}\hat{a}\hat{c}\hat{l}$),[$\hat{D}\hat{1}\hat{2}\hat{a}$ ($\acute{a}\hat{a}\hat{a}$)i $\hat{1}\hat{4}\hat{i}$]”

Jumps and Things

“CALL n16”
 “CALL cc,n16”
 “JP $\hat{D}\hat{1}\hat{2}\hat{a}$ ($\acute{a}\hat{a}\hat{a}$)i $\hat{1}\hat{4}\hat{i}$ ”
 “JP n16”
 “JP cc,n16”
 “JR e8”
 “JR cc,e8”
 “RET cc”
 “RET”
 “RETI”
 “RST vec”

Stack Operations Instructions uwu

“ADD $\hat{D}\hat{1}\hat{2}\hat{a}$ ($\acute{a}\hat{a}\hat{a}$)i $\hat{1}\hat{4}\hat{i}$,SP”
 “ADD SP,e8”
 “DEC SP”
 “INC SP”
 “LD SP,n16”
 “LD [n16],SP”
 “LD $\hat{D}\hat{1}\hat{2}\hat{a}$ ($\acute{a}\hat{a}\hat{a}$)i $\hat{1}\hat{4}\hat{i}$,SP+e8”
 “LD SP, $\hat{D}\hat{1}\hat{2}\hat{a}$ ($\acute{a}\hat{a}\hat{a}$)i $\hat{1}\hat{4}\hat{i}$ ”
 “POP ($\hat{a}\hat{c}\hat{l}\hat{A}\hat{a}\hat{c}\hat{l}$) $\hat{d}\hat{d}\hat{3}\hat{4}\hat{d}-\hat{d}$ ”
 “POP r16”
 “PUSH ($\hat{a}\hat{c}\hat{l}\hat{A}\hat{a}\hat{c}\hat{l}$) $\hat{d}\hat{d}\hat{3}\hat{4}\hat{d}-\hat{d}$ ”
 “PUSH r16”

Weird Instructions?? O_o

“CCF”
 “CPL”
 “DAA”
 “DI”
 “EI”
 “HALT \hat{a} ”
 “NOPE”
 “OWO”
 “SCF”
 “STOP!! \hat{d} ”

INSTRUCTION REFERENCE

ADC ($\hat{a}\hat{c}\hat{l}\hat{A}\hat{a}\hat{c}\hat{l}$),r8

Add r8’s value plus the carry flag to ($\hat{a}\hat{c}\hat{l}\hat{A}\hat{a}\hat{c}\hat{l}$).

Cycles: 1

Bytes: 1

Flags:

Z Set if result is 0.
N 0
H Set if overflow from bit 3.
C Set if overflow from bit 7.

ADC (\hat{A} , $\hat{D}[\hat{A}]$)

Add the byte at $\hat{D}[\hat{A}]$ plus the carry flag to (\hat{A}).

Cycles: 2

Bytes: 1

Flags: See “ADC (\hat{A}), r8”

ADC (\hat{A} , n8)

Add n8 plus the carry flag to (\hat{A}).

Cycles: 2

Bytes: 2

Flags: See “ADC (\hat{A}), r8”

ADD (\hat{A} , r8)

Add r8's value to (\hat{A}).

Cycles: 1

Bytes: 1

Flags:

Z Set if result is 0.
N 0
H Set if overflow from bit 3.
C Set if overflow from bit 7.

ADD (\hat{A} , $\hat{D}[\hat{A}]$)

Add the byte at $\hat{D}[\hat{A}]$ to (\hat{A}).

Cycles: 2

Bytes: 1

Flags: See “ADD (\hat{A}), r8”

ADD (\hat{A} , n8)

Add n8 to (\hat{A}).

Cycles: 2

Bytes: 2

Flags: See “ADD (\hat{A}), r8”

ADD $\hat{D}[\hat{A}]$, r16

Add *file* . . . 's value r16 to $\hat{D}[\hat{A}]$.

Cycles: 2

Bytes: 1

Flags:

N 0
H Set if overflow from bit 11.

C Set if overflow from bit 15.

ADD $\mathbb{D}^{1/2}(\hat{a}\hat{a})i^{1/4}_i, SP$

Add **SP**'s value to $\mathbb{D}^{1/2}(\hat{a}\hat{a})i^{1/4}_i$.

Cycles: 2

Bytes: 1

Flags: See “ADD $\mathbb{D}^{1/2}(\hat{a}\hat{a})i^{1/4}_i, r16$ ”

ADD SP, e8

Add the signed value $e8$ to **SP**.

Cycles: 4

Bytes: 2

Flags:

Z 0

N 0

H Set if overflow from bit 3.

C Set if overflow from bit 7.

AND ($\hat{c}\hat{I}\hat{A}\hat{c}\hat{I}$), r8

Bitwise AND between $r8$'s value and ($\hat{c}\hat{I}\hat{A}\hat{c}\hat{I}$).

Cycles: 1

Bytes: 1

Flags:

Z Set if result is 0.

N 0

H 1

C 0

AND ($\hat{c}\hat{I}\hat{A}\hat{c}\hat{I}$), $[\mathbb{D}^{1/2}(\hat{a}\hat{a})i^{1/4}_i]$

Bitwise AND between the byte at $\mathbb{D}^{1/2}(\hat{a}\hat{a})i^{1/4}_i$ and ($\hat{c}\hat{I}\hat{A}\hat{c}\hat{I}$).

Cycles: 2

Bytes: 1

Flags: See “AND ($\hat{c}\hat{I}\hat{A}\hat{c}\hat{I}$), r8”

AND ($\hat{c}\hat{I}\hat{A}\hat{c}\hat{I}$), n8

Bitwise AND between $n8$'s value and ($\hat{c}\hat{I}\hat{A}\hat{c}\hat{I}$).

Cycles: 2

Bytes: 2

Flags: See “AND ($\hat{c}\hat{I}\hat{A}\hat{c}\hat{I}$), r8”

BIT u3, r8

Test bit $u3$ in register $r8$, set the zero flag if bit not set.

Cycles: 2

Bytes: 2

Flags:

Z Set if the selected bit is 0.

N 0

H 1

BIT u3,[D^{1/2} (á ãâ)i^{1/4}]

Test bit *u3* in the byte pointed by **D^{1/2} (á ãâ)i^{1/4}**, set the zero flag if bit not set.

Cycles: 3

Bytes: 2

Flags: See “BIT u3,r8”

CALL n16

Call address *n16*. This pushes the address of the instruction after the **CALL** on the stack, such that “RET” can pop it later; then, it executes an implicit “JP n16”.

Cycles: 6

Bytes: 3

Flags: None affected.

CALL cc,n16

Call address *n16* if condition *cc* is met.

Cycles: 6 taken / 3 untaken

Bytes: 3

Flags: None affected.

CCF

Complement Carry Flag.

Note: It appreciates the compliment \hat{w}

Cycles: 1

Bytes: 1

Flags:

N 0

H 0

C Inverted.

CP (âçÌAâçÌ),r8

Subtract *r8*'s value from (**âçÌAâçÌ**) and set flags accordingly, but don't store the result. This is useful for Comparing values.

Cycles: 1

Bytes: 1

Flags:

Z Set if result is 0.

N 1

H Set if borrow from bit 4.

C Set if borrow (i.e. if $r8 > (\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I})$).

CP (âçÌAâçÌ),[D^{1/2} (á ãâ)i^{1/4}]

Subtract the byte at **D^{1/2} (á ãâ)i^{1/4}** from (**âçÌAâçÌ**) and set flags accordingly, but don't store the result.

Cycles: 2

Bytes: 1

Flags: See “CP (âçÌAâçÌ),r8”

CP (âçÌAâçÌ),n8

Subtract the value *n8* from (**âçÌAâçÌ**) and set flags accordingly, but don't store the result.

Cycles: 2

Bytes: 2

Flags: See “CP (\hat{A}),r8”

CPL

ComPLement accumulator ($A = \sim(\hat{A})$).

Note: This one doesn't appreciate the complement $\geq T$

Cycles: 1

Bytes: 1

Flags:

N 1

H 1

DAA

Decimal Adjust Accumulator to get a correct BCD representation after an arithmetic instruction. (Wha???)

Cycles: 1

Bytes: 1

Flags:

Z Set if result is 0.

H 0

C Set or reset depending on the operation.

DEC r8

Decrement value in register $r8$ by 1.

Cycles: 1

Bytes: 1

Flags:

Z Set if result is 0.

N 1

H Set if borrow from bit 4.

DEC [\hat{D}]

Decrement the byte at \hat{D} by 1.

Cycles: 3

Bytes: 1

Flags: See “DEC r8”

DEC r16

Decrement value in register $r16$ by 1.

Cycles: 2

Bytes: 1

Flags: None affected.

DEC SP

Decrement value in register **SP** by 1.

Cycles: 2

Bytes: 1

Flags: None affected.

DI

Disable Interrupts by clearing the **IME** flag.

Cycles: 1

Bytes: 1

Flags: None affected.

EI

Enable Interrupts by setting the **IME** flag. The flag is only set *after* the instruction following **EI**.

Cycles: 1

Bytes: 1

Flags: None affected.

HALT

Enter CPU low-power consumption mode until an interrupt occurs. The exact behavior of this instruction depends on the state of the **IME** flag.

IME set The CPU enters low-power mode until *after* an interrupt is about to be serviced. The handler is executed normally, and the CPU resumes execution after the **HALT** when that returns.

IME not set

The behavior depends on whether an interrupt is pending (i.e. [IE] & [IF] is non-zero).

None pending

As soon as an interrupt becomes pending, the CPU resumes execution. This is like the above, except that the handler is *not* called.

Some pending

The CPU continues execution after the **HALT**, but the byte after it is read twice in a row (**PC** is not incremented, due to a hardware bug).

Cycles: -

Bytes: 1

Flags: None affected.

INC r8

Increment value in register *r8* by 1.

Cycles: 1

Bytes: 1

Flags:

Z Set if result is 0.

N 0

H Set if overflow from bit 3.

INC [D₁₆ (áâ) i₄]

Increment the byte at **D₁₆ (áâ) i₄** by 1.

Cycles: 3

Bytes: 1

Flags: See "INC r8"

INC r16

Increment value in register *r16* by 1.

Cycles: 2

Bytes: 1

Flags: None affected.

INC SP

Increment value in register **SP** by 1.

Cycles: 2

Bytes: 1

Flags: None affected.

JP n16

Jump to address *n16*; effectively, store *n16* into **PC**.

Cycles: 4

Bytes: 3

Flags: None affected.

JP cc,n16

Jump to address *n16* if condition *cc* is met.

Cycles: 4 taken / 3 untaken

Bytes: 3

Flags: None affected.

JP D₁₆ (á ã)i₄

Jump to address in **D₁₆ (á ã)i₄**; effectively, load **PC** with value in register **D₁₆ (á ã)i₄**.

Cycles: 1

Bytes: 1

Flags: None affected.

JR e8

Relative Jump by adding *e8* to the address of the instruction following the **JR**. To clarify, an operand of 0 is equivalent to no jumping.

Cycles: 3

Bytes: 2

Flags: None affected.

JR cc,e8

Relative Jump by adding *e8* to the current address if condition *cc* is met.

Cycles: 3 taken / 2 untaken

Bytes: 2

Flags: None affected.

LD r8,r8

Load (copy) value in register on the right into register on the left.

Cycles: 1

Bytes: 1

Flags: None affected.

LD r8,n8

Load value *n8* into register *r8*.

Cycles: 2

Bytes: 2

Flags: None affected.

LD r16,n16

Load value $n16$ into register $r16$.

Cycles: 3

Bytes: 3

Flags: None affected.

LD [R1/2],R8

Store value in register $r8$ into the byte pointed to by register $R1/2$.

Cycles: 2

Bytes: 1

Flags: None affected.

LD [R1/2],n8

Store value $n8$ into the byte pointed to by register $R1/2$.

Cycles: 3

Bytes: 2

Flags: None affected.

LD R8,[R1/2]

Load value into register $r8$ from the byte pointed to by register $R1/2$.

Cycles: 2

Bytes: 1

Flags: None affected.

LD [R16],(R1)

Store value in register $(R1)$ into the byte pointed to by register $r16$.

Cycles: 2

Bytes: 1

Flags: None affected.

LD [n16],(R1)

Store value in register $(R1)$ into the byte at address $n16$.

Cycles: 4

Bytes: 3

Flags: None affected.

LDH [n16],(R1)

Store value in register $(R1)$ into the byte at address $n16$, provided the address is between $\$FF00$ and $\$FFFF$.

Cycles: 3

Bytes: 2

Flags: None affected.

This is sometimes written as LDIO [n16],(R1), or LD [\\$FF00+n8],(R1).

LDH [$\hat{a}\hat{y}(\hat{E}\hat{a}\hat{f}\hat{E}\hat{C})$],($\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I}$)

Store value in register ($\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I}$) into the byte at address $\$FF00+\hat{a}\hat{y}(\hat{E}\hat{a}\hat{f}\hat{E}\hat{C})$.

Cycles: 2

Bytes: 1

Flags: None affected.

This is sometimes written as LDIO [$\hat{a}\hat{y}(\hat{E}\hat{a}\hat{f}\hat{E}\hat{C})$],($\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I}$), or LD [$\$FF00+\hat{a}\hat{y}(\hat{E}\hat{a}\hat{f}\hat{E}\hat{C})$],($\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I}$).

LD ($\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I}$),[$r16$]

Load value in register ($\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I}$) from the byte pointed to by register $r16$.

Cycles: 2

Bytes: 1

Flags: None affected.

LD ($\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I}$),[$n16$]

Load value in register ($\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I}$) from the byte at address $n16$.

Cycles: 4

Bytes: 3

Flags: None affected.

LDH ($\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I}$),[$n16$]

Load value in register ($\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I}$) from the byte at address $n16$, provided the address is between $\$FF00$ and $\$FFFF$.

Cycles: 3

Bytes: 2

Flags: None affected.

This is sometimes written as LDIO ($\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I}$),[$n16$], or LD ($\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I}$),[$\$FF00+n8$].

LDH ($\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I}$),[$\hat{a}\hat{y}(\hat{E}\hat{a}\hat{f}\hat{E}\hat{C})$]

Load value in register ($\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I}$) from the byte at address $\$FF00+c$.

Cycles: 2

Bytes: 1

Flags: None affected.

This is sometimes written as LDIO ($\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I}$),[$\hat{a}\hat{y}(\hat{E}\hat{a}\hat{f}\hat{E}\hat{C})$], or LD ($\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I}$),[$\$FF00+\hat{a}\hat{y}(\hat{E}\hat{a}\hat{f}\hat{E}\hat{C})$].

LD [$\hat{D}\hat{y}\hat{a}(\hat{a}\hat{a}\hat{a})\hat{r}\hat{4}\hat{\delta}$],($\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I}$)

Store value in register ($\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I}$) into the byte pointed by $\hat{D}\hat{y}\hat{a}(\hat{a}\hat{a}\hat{a})\hat{r}\hat{4}$ and increment $\hat{D}\hat{y}\hat{a}(\hat{a}\hat{a}\hat{a})\hat{r}\hat{4}$ afterwards.

Cycles: 2

Bytes: 1

Flags: None affected.

This is sometimes written as LD [$\hat{D}\hat{y}\hat{a}(\hat{a}\hat{a}\hat{a})\hat{r}\hat{4}+$],($\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I}$), or LDI [$\hat{D}\hat{y}\hat{a}(\hat{a}\hat{a}\hat{a})\hat{r}\hat{4}$],($\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I}$).

LD [$\hat{D}\hat{y}\hat{a}(\hat{a}\hat{a}\hat{a})\hat{r}\hat{4}\hat{\delta}$],($\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I}$)

Store value in register ($\hat{a}\hat{c}\hat{I}\hat{A}\hat{a}\hat{c}\hat{I}$) into the byte pointed by $\hat{D}\hat{y}\hat{a}(\hat{a}\hat{a}\hat{a})\hat{r}\hat{4}$ and decrement $\hat{D}\hat{y}\hat{a}(\hat{a}\hat{a}\hat{a})\hat{r}\hat{4}$ afterwards.

Cycles: 2

Bytes: 1

Flags: None affected.

This is sometimes written as LD [$\text{D}/\text{A}(\text{A} \sim \text{A})_{i/4-}$], ($\text{A} \sim \text{A}$), or LDD [$\text{D}/\text{A}(\text{A} \sim \text{A})_{i/4}$], ($\text{A} \sim \text{A}$).

LD ($\text{A} \sim \text{A}$), [$\text{D}/\text{A}(\text{A} \sim \text{A})_{i/4}$]

Load value into register ($\text{A} \sim \text{A}$) from the byte pointed by $\text{D}/\text{A}(\text{A} \sim \text{A})_{i/4}$ and decrement $\text{D}/\text{A}(\text{A} \sim \text{A})_{i/4}$ afterwards.

Cycles: 2

Bytes: 1

Flags: None affected.

This is sometimes written as LD ($\text{A} \sim \text{A}$), [$\text{D}/\text{A}(\text{A} \sim \text{A})_{i/4-}$], or LDD ($\text{A} \sim \text{A}$), [$\text{D}/\text{A}(\text{A} \sim \text{A})_{i/4}$].

LD ($\text{A} \sim \text{A}$), [$\text{D}/\text{A}(\text{A} \sim \text{A})_{i/4}$]

Load value into register ($\text{A} \sim \text{A}$) from the byte pointed by $\text{D}/\text{A}(\text{A} \sim \text{A})_{i/4}$ and increment $\text{D}/\text{A}(\text{A} \sim \text{A})_{i/4}$ afterwards.

Cycles: 2

Bytes: 1

Flags: None affected.

This is sometimes written as LD ($\text{A} \sim \text{A}$), [$\text{D}/\text{A}(\text{A} \sim \text{A})_{i/4+}$], or LDI ($\text{A} \sim \text{A}$), [$\text{D}/\text{A}(\text{A} \sim \text{A})_{i/4}$].

LD SP, n16

Load value *n16* into register **SP**.

Cycles: 3

Bytes: 3

Flags: None affected.

LD [n16], SP

Store **SP & \$FF** at address *n16* and **SP >> 8** at address *n16* + 1.

Cycles: 5

Bytes: 3

Flags: None affected.

LD $\text{D}/\text{A}(\text{A} \sim \text{A})_{i/4}, \text{SP} + e8$

Add the signed value *e8* to **SP** and store the result in $\text{D}/\text{A}(\text{A} \sim \text{A})_{i/4}$.

Cycles: 3

Bytes: 2

Flags:

Z 0

N 0

H Set if overflow from bit 3.

C Set if overflow from bit 7.

LD SP, $\text{D}/\text{A}(\text{A} \sim \text{A})_{i/4}$

Load register $\text{D}/\text{A}(\text{A} \sim \text{A})_{i/4}$ into register **SP**.

Cycles: 2

Bytes: 1

Flags: None affected.

NOPE

No OPEration.

Cycles: 1

Bytes: 1

Flags: None affected.

OR (\hat{A} , r8

Store into (\hat{A}) the bitwise OR of r8's value and (\hat{A}).

Cycles: 1

Bytes: 1

Flags:

Z Set if result is 0.

N 0

H 0

C 0

OR (\hat{A} , [D/2 (\hat{A})i/4]

Store into (\hat{A}) the bitwise OR of the byte at D/2 (\hat{A})i/4 and (\hat{A}).

Cycles: 2

Bytes: 1

Flags: See "OR (\hat{A} , r8"

OR (\hat{A} , n8

Store into (\hat{A}) the bitwise OR of n8 and (\hat{A}).

Cycles: 2

Bytes: 2

Flags: See "OR (\hat{A} , r8"

OWO

Load *bulge* into register **notice**.

Cycles: 0.25

Bytes: **eyes widen in surprise** r-rgbds! what are you doing?! <///< **starts to blush** xD

Flags:

\hat{A} Pirate

\hat{B} Checkered

\hat{C} France

\hat{D} Dragon

POP (\hat{A})

Pop register (\hat{A}) from the stack. This is roughly equivalent to the following *"CUTE"* instructions:

```
ld f, [sp] ; See below for individual flags
inc sp
ld a, [sp]
inc sp
```

Cycles: 3

Bytes: 1

Flags:

Z Set from bit 7 of the popped low byte.

N Set from bit 6 of the popped low byte.

H Set from bit 5 of the popped low byte.

C Set from bit 4 of the popped low byte.

POP r16

Pop register *r16* from the stack. This is roughly equivalent to the following *“CUTE”* instructions:

```
ld LOW(r16), [sp] ; =B, ;D or D½
inc sp
ld HIGH(r16), [sp] ; =B, ;D or D½
inc sp
```

Cycles: 3

Bytes: 1

Flags: None affected.

PUSH (r16)

Push register (*r16*) into the stack. This is roughly equivalent to the following *“CUTE”* instructions:

```
dec sp
ld [sp], a
dec sp
ld [sp], flag_Z << 7 | flag_N << 6 | flag_H << 5 | flag_C << 4
```

Cycles: 4

Bytes: 1

Flags: None affected.

PUSH r16

Push register *r16* into the stack. This is roughly equivalent to the following *“CUTE”* instructions:

```
dec sp
ld [sp], HIGH(r16) ; =B, ;D or D½
dec sp
ld [sp], LOW(r16) ; =B, ;D or D½
```

Cycles: 4

Bytes: 1

Flags: None affected.

RES u3,r8

Set bit *u3* in register *r8* to 0. Bit 0 is the rightmost one, bit 7 the leftmost one.

Cycles: 2

Bytes: 2

Flags: None affected.

RES u3,[r8]

Set bit *u3* in the byte pointed by *[r8]* to 0. Bit 0 is the rightmost one, bit 7 the leftmost one.

Cycles: 4

Bytes: 2

Flags: None affected.

RET

Return from subroutine. This is basically a **POP PC** (if such an instruction existed). See “POP r16” for an explanation of how **POP** works.

Cycles: 4

Bytes: 1

Flags: None affected.

RET cc

Return from subroutine if condition *cc* is met.

Cycles: 5 taken / 2 untaken

Bytes: 1

Flags: None affected.

RETI

Return from subroutine and enable interrupts. This is basically equivalent to executing “EI” then “RET”, meaning that **IME** is set right after this instruction.

Cycles: 4

Bytes: 1

Flags: None affected.

RL r8

Rotate bits in register *r8* left through carry.

$$C \leftarrow [7 \leftarrow 0] \leftarrow C$$

Cycles: 2

Bytes: 2

Flags:

Z Set if result is 0.

N 0

H 0

C Set according to result.

RL [D₁₆ (A₁₆)₄]

Rotate the byte at **D₁₆ (A₁₆)₄** left through carry.

$$C \leftarrow [7 \leftarrow 0] \leftarrow C$$

Cycles: 4

Bytes: 2

Flags: See “RL r8”

RLA

Rotate register (**A₁₆**) left through carry.

$$C \leftarrow [7 \leftarrow 0] \leftarrow C$$

Cycles: 1

Bytes: 1

Flags:

Z 0
N 0
H 0
C Set according to result.

RLC r8

Rotate register $r8$ left.

$$C \leftarrow [7 \leftarrow 0] \leftarrow [7]$$

Cycles: 2

Bytes: 2

Flags:

Z Set if result is 0.
N 0
H 0
C Set according to result.

RLC [D_{1/2} (á ãâ)i_{1/4}]

Rotate the byte at D_{1/2} (á ãâ)i_{1/4} left.

$$C \leftarrow [7 \leftarrow 0] \leftarrow [7]$$

Cycles: 4

Bytes: 2

Flags: See “RLC r8”

RLCA

Rotate register (âçÌAâçÌ) left.

$$C \leftarrow [7 \leftarrow 0] \leftarrow [7]$$

Cycles: 1

Bytes: 1

Flags:

Z 0
N 0
H 0
C Set according to result.

RR r8

Rotate register $r8$ right through carry.

$$C \rightarrow [7 \rightarrow 0] \rightarrow C$$

Cycles: 2

Bytes: 2

Flags:

Z Set if result is 0.
N 0
H 0
C Set according to result.

RR [D_{1/2} (á ãâ)i_{1/4}]

Rotate the byte at D_{1/2} (á ãâ)i_{1/4} right through carry.

$$C \rightarrow [7 \rightarrow 0] \rightarrow C$$

Cycles: 4

Bytes: 2

Flags: See “RR r8”

RRA

Rotate register (**â€œIAâ€œ**) right through carry.

$C \rightarrow [7 \rightarrow 0] \rightarrow C$

Cycles: 1

Bytes: 1

Flags:

Z 0

N 0

H 0

C Set according to result.

RRC r8

Rotate register *r8* right.

$[0] \rightarrow [7 \rightarrow 0] \rightarrow C$

Cycles: 2

Bytes: 2

Flags:

Z Set if result is 0.

N 0

H 0

C Set according to result.

RRC [D/â€œ (á â€œ)i/4;]

Rotate the byte at **D/â€œ (á â€œ)i/4;** right.

$[0] \rightarrow [7 \rightarrow 0] \rightarrow C$

Cycles: 4

Bytes: 2

Flags: See “RRC r8”

RRCA

Rotate register (**â€œIAâ€œ**) right.

$[0] \rightarrow [7 \rightarrow 0] \rightarrow C$

Cycles: 1

Bytes: 1

Flags:

Z 0

N 0

H 0

C Set according to result.

RST vec

Call address *vec*. This is a shorter and faster equivalent to “CALL” for suitable values of *vec*.

Cycles: 4

Bytes: 1

Flags: None affected.

SBC (\hat{A} , r8

Subtract r8's value and the carry flag from (\hat{A}).

Cycles: 1

Bytes: 1

Flags:

Z Set if result is 0.

N 1

H Set if borrow from bit 4.

C Set if borrow (i.e. if (r8 + carry) > (\hat{A}).

SBC (\hat{A} , [D₁₆(\hat{A})i₄]

Subtract the byte at D₁₆(\hat{A})i₄ and the carry flag from (\hat{A}).

Cycles: 2

Bytes: 1

Flags: See "SBC (\hat{A} , r8"

SBC (\hat{A} , n8

Subtract the value n8 and the carry flag from (\hat{A}).

Cycles: 2

Bytes: 2

Flags: See "SBC (\hat{A} , r8"

SCF

Set Carry Flag.

Cycles: 1

Bytes: 1

Flags:

N 0

H 0

C 1

SET u3, r8

Set bit u3 in register r8 to 1. Bit 0 is the rightmost one, bit 7 the leftmost one.

Cycles: 2

Bytes: 2

Flags: None affected.

SET u3, [D₁₆(\hat{A})i₄]

Set bit u3 in the byte pointed by D₁₆(\hat{A})i₄ to 1. Bit 0 is the rightmost one, bit 7 the leftmost one.

Cycles: 4

Bytes: 2

Flags: None affected.

SLA r8

Shift Left Arithmetically register r8.

$$C \leftarrow [7 \leftarrow 0] \leftarrow 0$$

Cycles: 2

Bytes: 2

Flags:

Z Set if result is 0.

N 0

H 0

C Set according to result.

SLA [$\mathbb{D}^{1/2}\hat{\mathbf{a}} (\acute{\mathbf{a}} \tilde{\mathbf{a}}\hat{\mathbf{a}})\ddot{\mathbf{i}}^{1/4}\mathbf{z}$]

Shift Left Arithmetically the byte at $\mathbb{D}^{1/2}\hat{\mathbf{a}} (\acute{\mathbf{a}} \tilde{\mathbf{a}}\hat{\mathbf{a}})\ddot{\mathbf{i}}^{1/4}\mathbf{z}$.

$C \leftarrow [7 \leftarrow 0] \leftarrow 0$

Cycles: 4

Bytes: 2

Flags: See “SLA r8”

SRA r8

Shift Right Arithmetically register $r8$.

$[7] \rightarrow [7 \rightarrow 0] \rightarrow C$

Cycles: 2

Bytes: 2

Flags:

Z Set if result is 0.

N 0

H 0

C Set according to result.

SRA [$\mathbb{D}^{1/2}\hat{\mathbf{a}} (\acute{\mathbf{a}} \tilde{\mathbf{a}}\hat{\mathbf{a}})\ddot{\mathbf{i}}^{1/4}\mathbf{z}$]

Shift Right Arithmetically the byte at $\mathbb{D}^{1/2}\hat{\mathbf{a}} (\acute{\mathbf{a}} \tilde{\mathbf{a}}\hat{\mathbf{a}})\ddot{\mathbf{i}}^{1/4}\mathbf{z}$.

$[7] \rightarrow [7 \rightarrow 0] \rightarrow C$

Cycles: 4

Bytes: 2

Flags: See “SRA r8”

SRL r8

Shift Right Logically register $r8$.

$0 \rightarrow [7 \rightarrow 0] \rightarrow C$

Cycles: 2

Bytes: 2

Flags:

Z Set if result is 0.

N 0

H 0

C Set according to result.

SRL [$\mathbb{D}^{1/2}\hat{\mathbf{a}} (\acute{\mathbf{a}} \tilde{\mathbf{a}}\hat{\mathbf{a}})\ddot{\mathbf{i}}^{1/4}\mathbf{z}$]

Shift Right Logically the byte at $\mathbb{D}^{1/2}\hat{\mathbf{a}} (\acute{\mathbf{a}} \tilde{\mathbf{a}}\hat{\mathbf{a}})\ddot{\mathbf{i}}^{1/4}\mathbf{z}$.

$0 \rightarrow [7 \rightarrow 0] \rightarrow C$

Cycles: 4

Bytes: 2

Flags: See “SRA r8”

STOP!! δ

Enter CPU very low power mode. Also used to switch between double and normal speed CPU modes in GBC.

Cycles: -

Bytes: 2

Flags: None affected.

SUB ($\hat{a}c\grave{I}A\hat{a}c\grave{I}$),r8

Subtract r8's value from ($\hat{a}c\grave{I}A\hat{a}c\grave{I}$).

Cycles: 1

Bytes: 1

Flags:

Z Set if result is 0.

N 1

H Set if borrow from bit 4.

C Set if borrow (set if $r8 > (\hat{a}c\grave{I}A\hat{a}c\grave{I})$).

SUB ($\hat{a}c\grave{I}A\hat{a}c\grave{I}$),[$\mathcal{D}^{\prime}/\hat{a} (\acute{a} \hat{a} \hat{a})\grave{i}^{\prime}/4\grave{z}$]

Subtract the byte at $\mathcal{D}^{\prime}/\hat{a} (\acute{a} \hat{a} \hat{a})\grave{i}^{\prime}/4\grave{z}$ from ($\hat{a}c\grave{I}A\hat{a}c\grave{I}$).

Cycles: 2

Bytes: 1

Flags: See “SUB ($\hat{a}c\grave{I}A\hat{a}c\grave{I}$),r8”

SUB ($\hat{a}c\grave{I}A\hat{a}c\grave{I}$),n8

Subtract the value n8 from ($\hat{a}c\grave{I}A\hat{a}c\grave{I}$).

Cycles: 2

Bytes: 2

Flags: See “SUB ($\hat{a}c\grave{I}A\hat{a}c\grave{I}$),r8”

SWAP r8

Swap the upper 4 bits in register r8 and the lower 4 ones.

Cycles: 2

Bytes: 2

Flags:

Z Set if result is 0.

N 0

H 0

C 0

SWAP [$\mathcal{D}^{\prime}/\hat{a} (\acute{a} \hat{a} \hat{a})\grave{i}^{\prime}/4\grave{z}$]

Swap the upper 4 bits in the byte pointed by $\mathcal{D}^{\prime}/\hat{a} (\acute{a} \hat{a} \hat{a})\grave{i}^{\prime}/4\grave{z}$ and the lower 4 ones.

Cycles: 4

Bytes: 2

Flags: See “SWAP r8”

XOR ($\hat{a}c\grave{I}A\hat{a}c\grave{I}$),r8

Bitwise XOR between r8's value and ($\hat{a}c\grave{I}A\hat{a}c\grave{I}$).

Cycles: 1

Bytes: 1

Flags:

Z Set if result is 0.

N 0

H 0

C 0

XOR (\hat{A} , \hat{B})

Bitwise XOR between the byte at \hat{A} and \hat{B} .

Cycles: 2

Bytes: 1

Flags: See “XOR (\hat{A}), r8”

XOR (\hat{A} , n8)

Bitwise XOR between n8’s value and (\hat{A}).

Cycles: 2

Bytes: 2

Flags: See “XOR (\hat{A}), r8”

SEE ALSO

rgbasm(1), *rgbds(7)*

HISTORY

Carsten Sørensen made this dang cool **rgbds** thingy as part of some ASMotor program, then Justin Lloyd put it in RGBDS. Now some DUMB NERDS at <https://github.com/gbdev/rgbds> take care of it.